(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 462 328 A1**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **90201602.1**

(51) Int. Cl.[5]: **G06F 11/26**, G01R 31/318

(22) Date of filing: **18.06.90**

(43) Date of publication of application:
27.12.91 Bulletin 91/52

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IT LI LU NL SE

(71) Applicant: **BELL TELEPHONE MANUFACTURING COMPANY Naamloze Vennootschap**
Francis Wellesplein 1
B-2000 Antwerp(BE)

(72) Inventor: **Huyskens, Erik**
Pastoor Van Loenhoutlaan 2
B-2140 Westmalle(BE)
Inventor: **Reusens, Peter Paul Frans**
Warande 121
B-9270 Laarne(BE)
Inventor: **Swerts, Urbain**
Pater Renaat De Vosstraat 52
B-2520 Mortsel(BE)

(74) Representative: **Vermeersch, Robert et al**
BELL TELEPHONE MANUFACTURING COMPANY Naamloze Vennootschap Patent Department Francis Wellesplein 1
B-2018 Antwerpen(BE)

(54) Test device for an electronic chip.

(57) A test device (TD1, SC1) operating in emulation mode for functionally replacing a processor (DSP1) of an integrated electronic chip (EC) by an emulating processor (DSP2) coupled thereto via a first scan path (SC1) built arround the processor (DSP1) and accesible via only two terminals (I, O) of the chip. The first scan path is constituted by a string of cells (CC1) connected in series between the two terminals, each cell latching a data bit normally transferred from another circuit, also built on the chip, to the processor thereof. The latched data is then serially transferred to a second scan path (SC2) similar to the first one and built arround the emulating processor. From the second scan path, the data is transmitted to the emulating processor which handles it and returns resulting data to this second scan path. This resulting data is then transferred back to the first scan path from which it is supplied to the other circuit. The transfer of data between the first and second scan paths is performed between each processing step of the emulating processor so that the test is executed in "real time".

A variant (TD2, SC1) of this test device discloses the substitution of the emulation processor (DSP2) for an observation processor (DSP3) provided with a third scan path (SC3) built arround it. This test device has a comparator (CMP) for comparing the the results of the observation processor (DSP3) and applied to the third scan path with those of the processor (DSP1) of the chip and available on the second scan path (SC2).

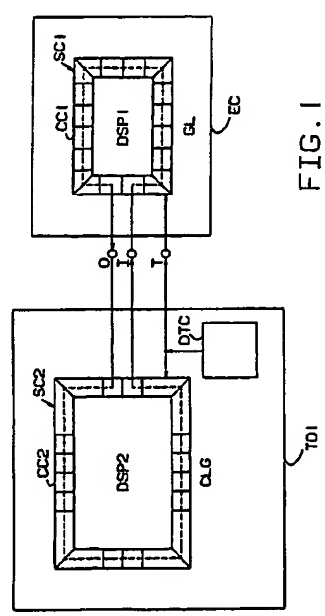


FIG. 1

EP 0 462 328 A1

The present invention relates to a test device for testing an integrated electronic chip including first processor means, said test device including interface means for interfacing said first processor means with other circuits, and second processor means coupled to said first processor means.

Such a test device is generally known in the art as an emulator. Therein the first processor means are replaced by the second processor means which are for instance more performant than the first ones or include a different software programme. The purpose of this test device is to check the behaviour of the other circuits together with these second processor means.

When the electronic chip is for instance only constituted by the first processor means, the socket wherein this chip is plugged may be considered as the interface means and to replace these first processor means by the second processor means this chip is removed from the socket and replaced therein by a connector linked to the second processor means.

In this way the test may be executed with the second processor means running at their normal processing speed. This allows to detect errors appearing only at that processing speed. Moreover, the test is performed by using the same environment, i.e. the other circuits, as when the first procesor means are operating. Thus this test allows detecting errors which do not appear when it is performed in a specific test environment, e.g. when specific test vectors are applied to the interface means instead of using the running second processor means. Indeed, in the case of using test vectors it is almost impossible to provide all the situations which may occur when the processor means are running in their real environment.

Due to the evolution of technology the size of the processor means is now so small that one or more of the above mentioned other circuits may also be integrated on the same chip. As a result it becomes difficult to have access to the interface means, now constituted by "pins" of the first processor means, since these pins are not accessible at the outside of the chip.

A solution to this problem of access would be to connect all these pins to the easily accessible external terminals of the chip. However, this solution is to be rejected because of the then required large number of external terminals and connections between the first processor means and these external terminals.

An object of the present invention is to provide a test device of the type mentioned above for testing an electronic chip in case this chip also includes, additionally to the first processor means, at least one of the above mentioned other circuits and without drastically increasing the number of external terminals of this chip, while allowing the second processor means to run at their normal processing speed.

According to the invention this object is achieved due to the fact that at least one of said other circuits is built on said chip; that said interface means include a first scan path constituted by a string of first cells built on said chip and including serially connected first read buffer means, one in each first cell, able to latch data normally transferred between said one circuit and said first processor means; that said test device further includes a second scan path constituted by a string of second cells and including serially connected second read buffer means, one in each second cell, able to latch data transferred between said second processor means and said second scan path; that said first processor means are coupled to said second processor means via the serial interconnection of said first and second read buffer means; and that said test device also includes data transfer means able to serially transfer latched data from said first read buffer means to said second read buffer means, and vice versa, at a predetermined transfer rate such that one data transfer is performed at each processor step of said second processor means.

In this way, data which is normally transferred from the one circuit to the first processor means via the first cells - operating as a transparent device for this transfer - is also latched in the first buffer means of these cells and transferred to corresponding second buffers means from which it is then transmitted to the second processor means, or vice versa. Because the first and the second scan paths are connected in series, only two external terminals are required on the chip for tranferring data irrespective of the number of buffer means. Moreover, the rate of data transfer from the first to the second scan paths, and reciprocally, may be so chosen that the second processor means are allowed to run at their normal processing speed.

It is to be noted that a test device including a scan path built on a chip is already known in the art, e.g. from the European patent application EP 0.313.230-A2. This scan path has the shape of a ring constituted by a plurality of input/output or latching cells including buffers for isolating the core logic of the chip from the external terminals thereof. In this known test device, input data is first loaded in the cells and then transmitted to the core logic which is constituted by electronic logical gates. The output data resulting from the handling of the input data by the logical gates is then transmitted back to the cells and transferred to the external terminals of the chip. However, this electronic chip is not provided with processor means

associated with other circuits also built on the same chip or not. Thus with this test device there are no problems relating to the test of processor means running at their normal processing speed, i.e. to perform a functional test.

The present invention relates also to a test device for testing an integrated electronic chip carrying processor means.

Another object of the present invention is to provide a test device which observes the operations of the processor means of the chip while they operate in their real environment and run at their normal processing speed.

According to the invention, this other object is achieved due to the fact that said test device includes:

- interface means built on said chip for interfacing said processor means with other circuits and including a first scan path constituted by a string of first cells and including serially connected first read buffer means, one in each first cell, able to latch data normally transferred between said processor means and said circuits;
- second processor means substantially identical to the first mentioned processor means and running at the same processing speed;
- a second scan path constituted by a string of second cells and including serially connected second read buffer means, one in each second cell, able to latch data, said second read buffer means being serially interconnected with said first read buffer means;
- data transfer means able to serially transfer the latched data from said first read buffer means to said second read buffer means, and vice versa, at a predetermined transfer rate such that one data transfer is performed between said first and second read buffer means at each processor step of said first processor means;
- a third scan path constituted by a string of third cells and including serially connected third read buffer means, one in each third cell, able to latch data transferred between said second processor means and said third scan path; and
- comparator means able to compare, at each processor step, the data received in said third scan path from said second processor means with the data received in said second scan path from said first processor means.

In this way both the first and the second processor means may run at their normal processing speed and in a common environment which is the real environment of the first processor means, i.e. the other circuits. In other words, the test device acts as a so-called "watch-dog" able to give an alarm when the results of the operations of the first processor means are different from those of the second processor means.

It is to be noted that because the other circuits are used in common by the first and by the second processor means and that the latter only can communicate with these other circuits by means of the transfer of data between the first and the second scan paths, such a transfer has to be done at each processing step of the processor means and for instance not until a predefined breakpoint in their software programme is reached. Indeed, in this last case the second processing means are not able to communicate with the other circuits before such a breakpoint.

Another characteristic feature of this test device is that at least one of said circuits is built on said chip.

The above mentioned and other objects and features of the invention will become more apparent and the invention itself will be best understood by referring to the following description of an embodiment taken in conjunction with the accompanying drawings wherein:

Fig. 1 shows a best device according to the invention and including a test circuit TD1, scan paths SC1 and SC2 used for testing a processor DSP1 in emulation mode;

Fig. 2 shows an unidirectional cell UC which may be used as a cell CC1 of the scan path SC1 of Fig. 1;

Fig. 3 shows an bidirectional cell BC which may be used as a cell CC1 of the scan path SC1 of Fig. 1; and

Fig. 4 shows a variant TD2 of the test circuit TD1 of Fig. 1 for testing the processor DSP1 in observation mode.

Fig. 1 shows a test device comprising a test circuit TD1 and a scan path SC1 which is built on an integrated electronic chip EC which further includes a processor DSP1 and a so-called "GLUE" logic GL, i.e. other circuits such as interfaces, memories, etc ... The test circuit TD1 further includes a processor DSP2, control logic CLG (not described in detail here), another scan path SC2 serially connected to the scan path SC1 in order to allow the processor DSP2 to run in the real environment, i.e. with the same glue logic GL, as the processor DSP1, as will become clear later, and a data transfer circuit DTC.

The scan path SC1 is an interface between the processor DSP1 and the glue logic GL and is constituted by a string of serially connected cells, such as CC1, surrounding the processor DSP1. Each cell CC1 is either of the unidirectional or bidirectional type, i.e. able to transfer data bits unidirectionally from GL to DSP1 or from DSP1 to GL, or bidirectionally between GL and DSP1 in a

transparent way respectively. An unidirectional cell UC is shown in Fig. 2 and a bidirectional cell BC is represented in Fig. 3. The operation of both UC and BC will be explained in more detail later.

The scan path SC2 included in the test circuit TD1 is similar to the scan path SC1 built on the chip EC, i.e. it includes a same number of serially connected cells, such as CC2, and surrounds the processor DSP2.

Each cell, CC1 or CC2, includes a read buffer RB and a write buffer WB (both shown in the Figs. 2 and 3). The read buffer RB is able to latch a data bit transferred through the corresponding cell. For instance, when such a data bit is transferred between the glue logic GL and the processor DSP1 through the scan path SC1, this data bit may also be latched in the read buffer RB. The write buffer WB is able to latch a data bit to be transmitted, e.g., to the glue logic GL and/or to a processor DSP1 or DSP2. Hereby a data bit latched in a write buffer WB always passes first through the associated read buffer RB.

All the read buffers RB of a same scan path SC1 or SC2 are connected in series and each end of a scan path, i.e. the end of the string of cells CC1 or CC2, is connected to a corresponding end of the other scan path via a respective external terminal I or O of the chip EC. The read buffers RB of the two scan paths SC1 and SC2 are thus interconnected so as to form a ring.

The above mentioned data transfer circuit DTC of TD1 is connected directly to all the cells CC2 of the scan path SC2 and via a set of external terminals, generally indicated by T in Fig. 1, to all the cells CC1 of the scan path SC1. The data transfer circuit DTC generates control signals for shifting the data bits latched in the read buffers RB of the scan path SC1 to the read buffers of the scan path SC2, and vice versa.

The data transfer circuit DTC further also controls the transfer of data bits:

- from the glue logic GL to the read buffers RB of the cells CC1 of the scan path SC1;
- from the write buffers WB of the cells CC1 of the scan path SC1 to the glue logic GL;
- from the processor DSP2 to the read buffers RB of the cells CC2 of the scan path SC2;
- from the write buffers WB of the cells CC2 of the scan path SC2 to the processor DSP2; and, in case of a variant TD2 (described later) of the test circuit TD1 is used,
- from the processor DSP1 to the read buffers RB of the cells CC1 of the scan path SC1;
- from the write buffers WB of the cells CC1 of the scan path SC1 to the processor DSP1.

All these shifts and transfers of data bits through the cells occur by means of control signals TST, BOS, CLK, EOS and AB generated by DTC and described later in relation to the Figs. 2 and 3.

The purpose of the test device is to emulate the operation of the processor DSP1. During this test, the processor DSP1 of the chip EC is disconnected or isolated from the other circuits constituting its environment, i.e. from the glue logic GL, and functionally replaced by the processor DSP2 of TD1 in order to perform the requested emulation. The processor DSP2 may for instance be more performant than DSP1 and/or include a different software programme so that the behaviour of the other circuits together with this processor DSP2 may be checked.

The test device operates as follows.

During each processing step of the processor DSP2 a full exchange of data occurs between the read buffers RB of the scan path SC1 and those of the scan path SC2.

For instance, when during a processing step of DSP2 a data bit from the glue logic GL and intended for the - now disconnected - processor DSP1 passes through a cell CC1, this data bit is captured and latched in the read buffer RB of this cell CC1. Before the occurrence of the next following processing step of DSP2, this data bit is transferred to the read buffer RB of a corresponding cell CC2 of the scan path SC2. This transfer occurs under the control of the data transfer circuit DTC as mentioned above. In the cell CC2, the data bit is transmitted from the read buffer RB to the write buffer WB from where it is then transmitted to the processor DSP2 which is able to handle it.

If, simultaneously, the processor DSP2 intends for transfer a data bit to the glue logic GL, this data bit is first latched in the read buffer RB of a cell CC2 and then transferred to the read buffer RB of a corresponding cell CC1 in the scan path SC1. From this read buffer RB the data bit is transmitted to the write buffer WB of the cell CC1 and so further to the glue logic GL.

As already mentioned an unidirectional cell UC is shown in detail in Fig. 2. This cell UC is for instance used in the scan path SC1 for allowing the transfer of data bits from the glue logic GL to the processor DSP1. The cell UC is therefore provided with a first input GO on which the data bits from GL are received, and with a first output PI where the data bits intended for DSP1 are available. The cell UC further has a second input CI for receiving data bits from the read buffer RB of the preceding cell in the scan path SC1, and a second output CO for transmitting data bits to the read buffer RB of the next following cell in this scan path SC1. additionally to the read RB and write WB buffers which are each constituted by a D-flip flop, the cell UC includes two multiplexers MX1 and MX2.

The input GO is connected to a first input 0 of the multiplexer MX1 as well as to a first input 0 of

the multiplexer MX2, the output of MX1 being connected to the first output PI. The second input CI is connected to the D-input of the read buffer RB via the multiplexer MX2 and more particularly via a second input 1 thereof. The Q-output of RB is connected to the second output CO as well as to the D-input of the write buffer WB, the Q-output of the latter being connected to a second input 1 of the multiplexer MX1.

The above mentioned control signals TST, BOS, CLK and EOS which are generated by the data transfer circuit DTC (Fig. 1) are applied to the cell UC via the above mentioned set of external terminals T of the chip EC.

In more detail, the control signal TST is applied to the first multiplexer MX1 in order to select either the first 0 or the second 1 input thereof. When the control signal TST selects the first input 0 of MX1, a data bit applied by the glue logic GL to the input GO is transmitted to the processor DSP1 via the multiplexer MX1 and the output PI. The cell UC then acts as a transparent device for this data bit. It is to be noted that the same data bit is also applied to the input 0 of the multiplexer MX2. On the other hand when the control signal TST selects the input 1 of MX1, the data bit latched in the write buffer WB is then transferred to the processor DSP1 instead of a data bit coming from the glue logic GL via the input GO. This possibility is for instance used in the scan path SC2 when a data bit is transferred from a cell CC2 to the processor DSP2.

The control signal BOS is applied to the multiplexer MX2 for controlling the transfer of data bits to the read buffer RB and selects either the input 0 or 1 of this multiplexer MX2. When the control signal BOS selects the input 0 of MX2, the above data bit coming from GL via the input GO is transmitted to RB whilst when the input 1 of MX2 is selected, the data bit applied to the input CI of the cell UC is transmitted to RB. It is to be noted that since all the cells of a scan path are connected in series, the data bit applied at the input CI of one of these cells is coming from the preceding cell in this scan path.

The control signal CLK is a clock signal applied to the clock input CL of the read buffer RB. CLK controls the shift transfer rate of the data bits in the scan path, i.e. the rate at which the data bits are transmitted from the read buffer RB of a cell to the read buffer of the next following cell in this scan path. This clock signal CLK thus controls the above transfer of data bits from the scan path SC1 to the scan path SC2 and vice versa.

Finally, the control signal EOS is applied to the clock input CL of the write buffer WB and controls the latching of a data bit therein. In other words, the control signal EOS allows the data bit transmitted from the read buffer RB to the ouput CO to be latched in the write buffer WB, or inhibits this latching.

A bidirectional cell BC is shown in detail in Fig. 3. It is similar the above described cell UC. However, the multiplexer MX2 has been replaced by a multiplexer MX3 and an additional multiplexer MX4 is used. The cell BC also has a third input PO to which the data bits coming from the processor DSP1 - in the above example - are applied and a third output GI on which the data bits intended for the glue logic GL are available.

The multiplexer MX3 has inputs 0 and 1 connected as those of the multiplexer MX2 and a third input 2 to which the input PO is connected. This input PO is further connected to an input 0 of the multiplexer MX4 of which the ouput is connected to the output GI. The output of the write buffer WB, connected to the input 1 of the multiplexer MX1, is further also connected to an input 1 of the multiplexer MX4.

The data transfer circuit DTC is able to apply supplementary control signal AB to the multiplexer MX3 for selecting either the input 0 or 2 thereof when the control signal BOS also applied to MX3 selects the data bit coming from the input GO - or PO - to be applied to the read buffer RB.

The above mentioned control signal TST is also applied to the multiplexer MX4 in order to select either the input 0 for 1 thereof. When this control signal selects the input 0 of MX4, the cell BC acts as a transparant device for the data bits transmitted from the processor DSP1 to the glue logic GL via the input PO and the output GI respectively. On the other hand, when the control signal TST selects the input 1 of MX4, the data bit then latched in the write buffer WB is transmitted to the glue logic GL instead of the data bit applied to the input PO.

Fig. 4 shows a variant TD2 of the test circuit TD1 of Fig. 1. The test circuit TD2 is comparable to the test circuit TD1 wherein the "emulating" processor DSP2 is replaced by an "observating" processor DSP3. TD2 thus includes a processor DSP3 instead of the processor DSP2 of TD1, and additionaly includes a scan path SC3 which is also constituted by a string of cells, such as CC3, including a same number of cells as SC1 and SC2 and surroundig a processor DSP3, and a comparator CMP coupled to both the scan paths SC2 and SC3 for comparing the data bits latched in read buffers of corresponding cells CC2/ CC3 thereof.

This test circuit TD2 is used for testing the processor DSP1 in observation mode. In this mode, both the processor DSP1 on the chip EC and the identical processor DSP3 forming part of the test circuit TD2 simultaneously run with the same data and at the same normal processing speed and the results of their operations are permanently com-

pared in CMP. This test device may thus be seen as a "watch-dog" able to give an alarm when the results of DSP1 and DSP3 are not identical.

In this test device, a data bit generated by the glue logic GL and intended for the processor DSP1 is transmitted not only to the latter processor DSP1 via the scan path SC1 but also to the processor DSP3 via the scan path SC2 as described above. This means that both the processors DSP1 and DSP3 then receive the same data bit from the glue logic GL. Both these processors then handle this data bit - or data bits since the contents of all the cells CC1 is transferred to all the cells CC2 - and generate a resulting data bit. The resulting data bit of the processor DSP1 is applied to and latched in the read buffer RB of a cell CC1 of the scan path SC1, whilst that of the processor DSP3 is applied to and latched in the read buffer RB of a corresponding cell CC3 of the scan path SC3.

Owing to the transfer of the data bits between the scan paths SC1 and SC2, the data bit then latched in the read buffer RB of CC1 is also available in the read buffer RB of a corresponding cell CC2. The comparator CMP then reads the data bit latched in this read buffer RB of CC2 and the one latched in the read buffer RB of the corresponding cell CC3 and compares them. When these two data bits are different an alarm signal may be generated by the test circuit TD2.

It is to be noted that in case the transfer of the data bits between the scan paths SC1 and SC2 can not be completed within one processing step of the processor due to the high operating rate of the latter, it is possible to slow down the normal processing speed of this processor and still perform the requested test.

While the principles of the invention have been described above in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation on the scope of the invention.

Claims

1. Test device (TD1, SC1) for testing an integrated electronic chip (EC) including first processor means (DSP1), said test device including interface means (SC1) for interfacing said first processor means with other circuits (GL), and second processor means (DSP2) coupled to said first processor means, characterized
   - in that at least one (GL) of said other circuits is built on said chip (EC),
   - in that said interface means include a first scan path (SC1) constituted by a string of first cells (CC1) built on said chip and including serially connected first read buffer means (RB), one in each first cell (CC1), able to latch data normally transferred between said one circuit (GL) and said first processor means (DSP1),
   - in that said test device further includes a second scan path (SC2) constituted by a string of second cells (CC2) and including serially connected second read buffer means (RB), one in each second cell (CC2), able to latch data transferred between said second processor means (DSP2) and said second scan path,
   - in that said first processor means are coupled to said second processor means via the serial interconnection (O; I) of said first and second read buffer means, and
   - in that said test device also includes data transfer means (DTC) able to serially transfer latched data from said first read buffer means to said second read buffer means, and vice versa, at a predetermined transfer rate such that one data transfer is performed at each processor step of said second processor means.

2. Test device (TD1, SC1) according to claim 1, characterized in that each of said first cells (CC1) further includes first write buffer means (WB) able to latch data received from said first read buffer means (RB) prior to transmit it to said one circuit (GL).

3. Test device (TD2, SC1) for testing an integrated electronic chip (EC) carrying processor means (DSP1), characterized in that said test device (TD2, SC1) includes:
   - interface means (SC1) built on said chip for interfacing said processor means (DSP1) with other circuits (GL) and including a first scan path (SC1) constituted by a string of first cells (CC1) and including serially connected first read buffer means (RB), one in each first cell (CC1), able to latch data normally transferred between said processor means and said circuits (GL),
   - second processor means (DSP3) substantially identical to the first mentioned processor means and running at the same processing speed,
   - a second scan path (SC2) constituted by a string of second cells (CC2) and including serially connected second read buffer means (RB), one in each second cell (CC2), able to latch data, said second read buffer means being serially interconnected (O; I) with said first read buffer means,

- data transfer means (DTC) able to serially transfer the latched data from said first read buffer means to said second read buffer means, and vice versa, at a predetermined transfer rate such that one data transfer is performed between said first and second read buffer means at each processor step of said first processor means,
- a third scan path (SC3) constituted by a string of third cells (CC3) and including serially connected third read buffer means (RB), one in each third cell (CC3), able to latch data transferred between said second processor means and said third scan path, and
- comparator means (CMP) able to compare, at each processor step, the data received in said third scan path from said second processor means with the data received in said second scan path from said first processor means.

4. Test device (TD2, SC1) according to claim 10, characterized in that at least one (GL) of said circuits is built on said chip (EC).

5. Test device (TD2, SC1) according to claim 10, characterized in that said data latched in said first read buffer means (RB) of said first cells (CC1) is also normally transferred between said first processor means (DSP1) and said circuits (GL).

6. Test device (TD2, SC1) according to claim 10, characterized in that said third scan path (SC3) includes the same number of cells (CC3) as said first scan path (SC1).

7. Test device (TD1, TD2; SC1) according to claim 1 or 10, characterized in that each of said second cells (662) further includes second write buffer means (WB) able to latch data received from said second read buffer means (RB) prior to transmit it to said second processor means (DSP2; DSP3).

8. Test device (TD1, TD2; SC1) according to claim 1 or 10, characterized in that said second scan path (SC2) includes the same number of cells (CC2) as said first scan path (SC1).

9. Test device (TD1, TD2; SC1) according to claim 1 or 10, characterized in that the serial interconnection (O; I) between said first and second read buffer means (RB) is realized via two terminals (O; I) of said chip (EC), each of said terminals linking an end of said string of first cells (CC1) to a corresponding end of said string of second cells (CC2).

10. Test device (TD1, TD2; SC1) according to claim 1 or 11, characterized in that said interface means (SC1) are built on said chip (EC) between said first processor means (DSP1) and said one circuit (GL) and surround said first processor means.

11. Test device (TD1, TD2; SC1) according to claim 10, characterized in that said second scan path (SC2) surrounds said second processor means (DSP2; DSP3).

12. Test device (TD1, TD2; SC1) according to any of the previous claims, characterized in that each of said latched data is constituted by a bit.

13. Test device (TD1, TD2; SC1) according to any of the previous claims, characterized in that each of said buffer means (RB, WB) are constituted by a D-flip flop.

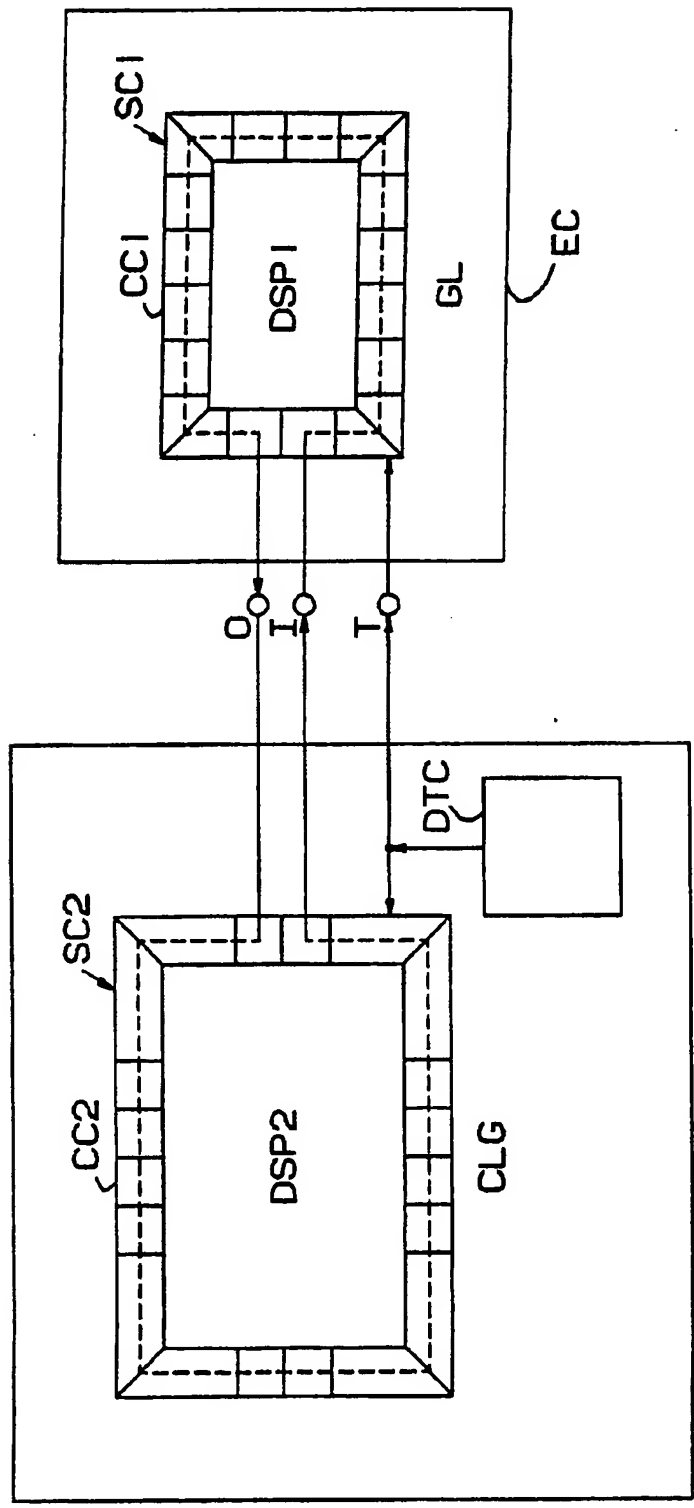


FIG. 1

FIG.2

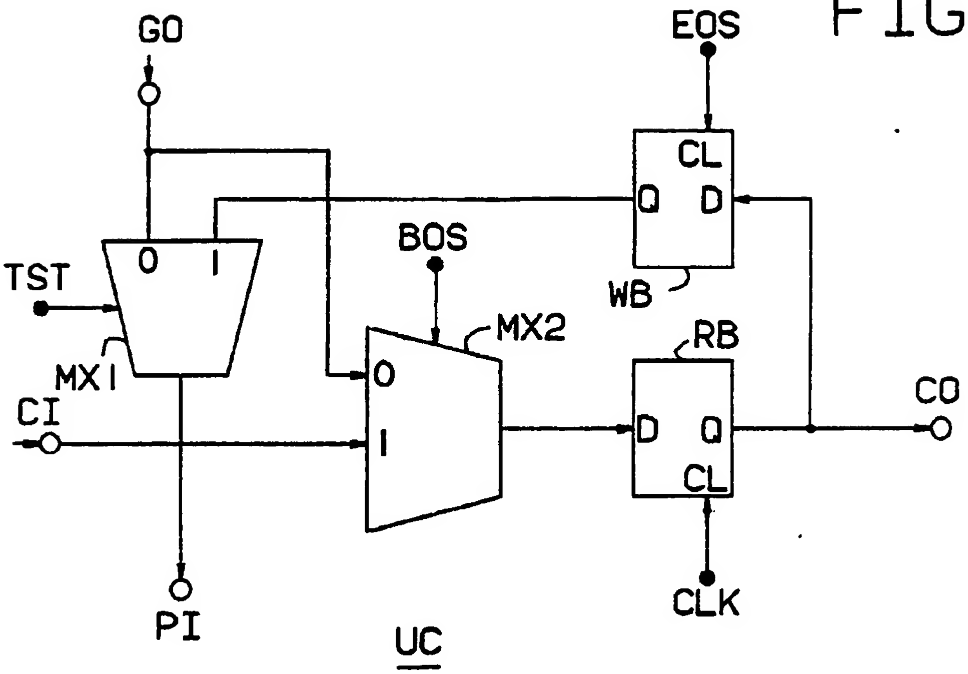
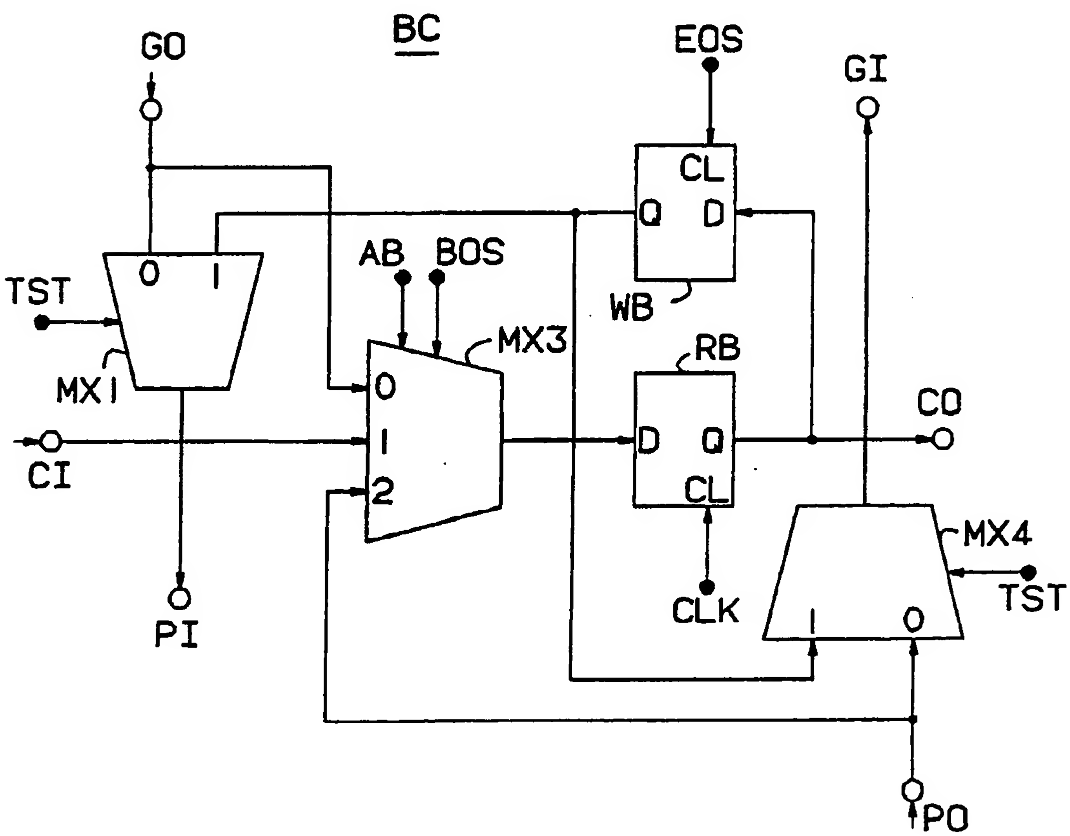

GO
EOS
CL
Q
D
TST
0
1
BOS
MX2
WB
RB
MX1
CI
0
1
D
Q
CL
CO
CLK
PI
UC

FIG.3


BC
GO
EOS
GI
CL
Q
D
TST
0
1
AB
BOS
MX3
WB
RB
MX1
0
1
2
D
Q
CL
CO
CI
MX4
TST
CLK
1
0
PI
PO

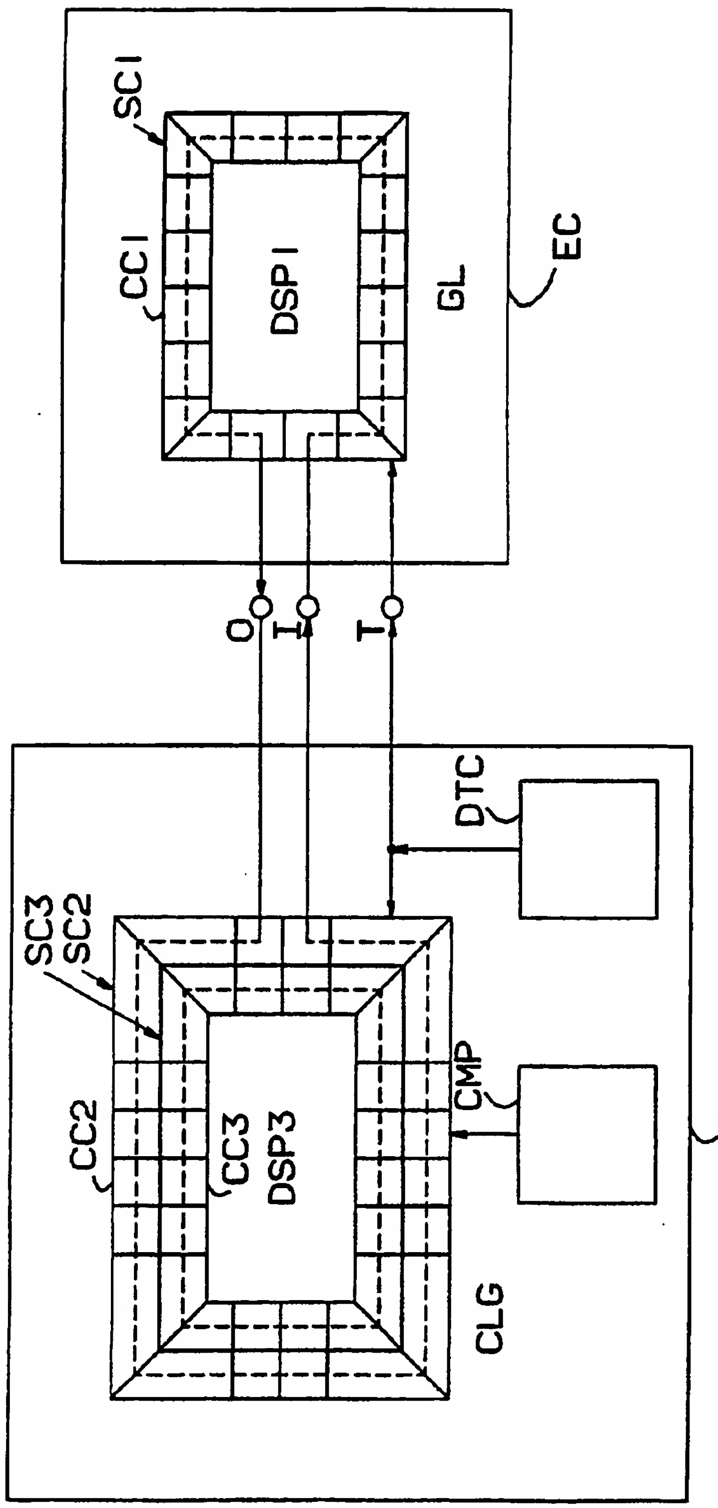


FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 20 1602

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 230 219 (IBM) * Abstract; column 1, line 3 - column 2, line 15; column 3, lines 1-42; column 5, lines 1-12 * - - -	1,3,12	G 06 F 11/26 G 01 R 31/318
A	TOUTE L'ELECTRONIQUE, no. 546, August/September 1989, pages 50-53; N.N.: "Le test de systèmes pour intégration de fonctions spécialisées" * Page 51, column 1, lines 1-41; page 51, column 2, line 48 - page 52, column 3, line 11; page 52, column 3, lines 30-39; page 53, figure 7 * - - -	1,2,12	
A	PROCEEDINGS OF THE 1987 INTERNATIONAL TEST CONFERENCE, Washington, DC, 1st - 3rd September 1987, pages 717-723; C. MAUNDER et al.: "Boundary-scan, a framework for structured design-for-test" * Page 715, column 1, line 12 - column 2, line 10; page 715, column 2, line 40 - page 717, column 1, line 8; page 719, column 2, line 53 - page 720, column 2, line 17; page 722, column 2, lines 1-29 * - - -	1-5,9,10, 12,13	
A	PROCEEDINGS OF THE IEEE 1989 CUSTOM INTEGRATED CIRCUITS CONFERENCE, San Diego, CA, 15th - 18th May 1989, pages 22.4.1 -22.4.4; P.P. FASANG: "Boundary scan and its application to analog-digital ASIC testing in a board/system enrivonment" * Page 22.4.1, column 2, line 29 - page 22.4.3, column 1, line 27 * - - -	1-5,9,10, 12,13	**TECHNICAL FIELDS SEARCHED (Int. Cl.5)** G 06 F 11/26
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 6, November 1980, page 2438, Armonk, US; L.L. HART et al.: "Circuit card diagnosis at machine speed" * Whole article, especialy pararaph 2 * - - - - -	3,6,8	

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
The Hague	21 January 91	HERREMAN,G.L.O.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
Y: particularly relevant if combined with another document of the same catagory
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention

E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document